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Adding Process Tailoring to Product Size for Better Cost Estimation

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Abstract

Adding Process Tailoring to Product Size for Better Cost Estimation

By David Bloom

Generally, when one is looking to create a parametric model to predict costs of an activity, then one looks to size relationships associated with that activity. For example, if one were to develop a parametric model for estimating the development of a Field Programmable Gate Array (FPGA), then, because most of the work to complete an FPGA revolves around software code development, building a parametric model around new code, modified code and reused code (with other size relationships) would probably be a good place to start.

However, as many aerospace organizations are incorporating the Capability Maturity Model Integration (CMMI) approach to process improvement, there is now substantially more development activity information available to parametric model development than just size (size being the number of lines of FPGA code). Further, there are normally pre-tailored process lists for any product type associated with an end application (such as manned flight FPGAs or space FPGAs).

This paper looks at the ability to incorporate repeatable processes into simple parametric models in order to improve the predictive capability. This paper will not be a rigorous mathematical approach into Bayesian statistics, but will be focus on the simple concepts of associating the effort to improve process repeatability that many aerospace organizations have made to become CMMI level 5 compliant with the ability to improve cost estimation practices.

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Agenda

- Introduction
- Example of cost prediction using only sizing elements
- Introduction to development processes
- Detailed look at work products
- Results

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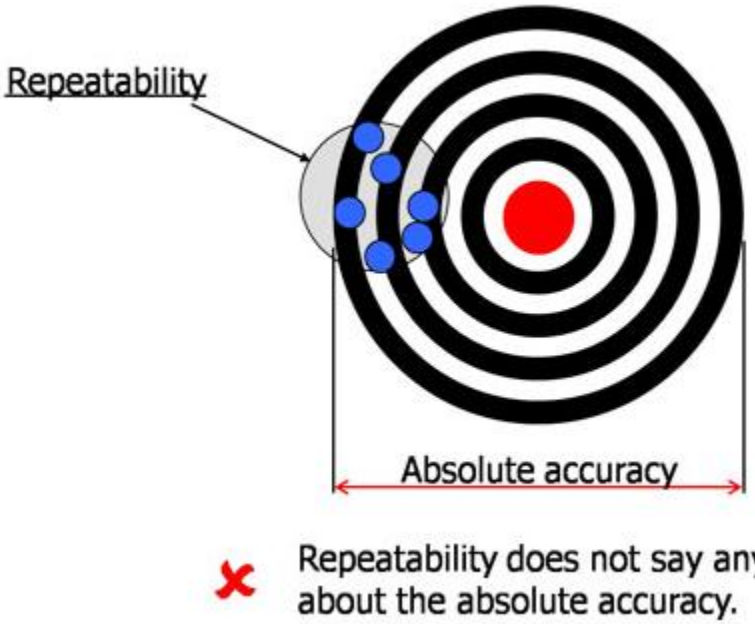
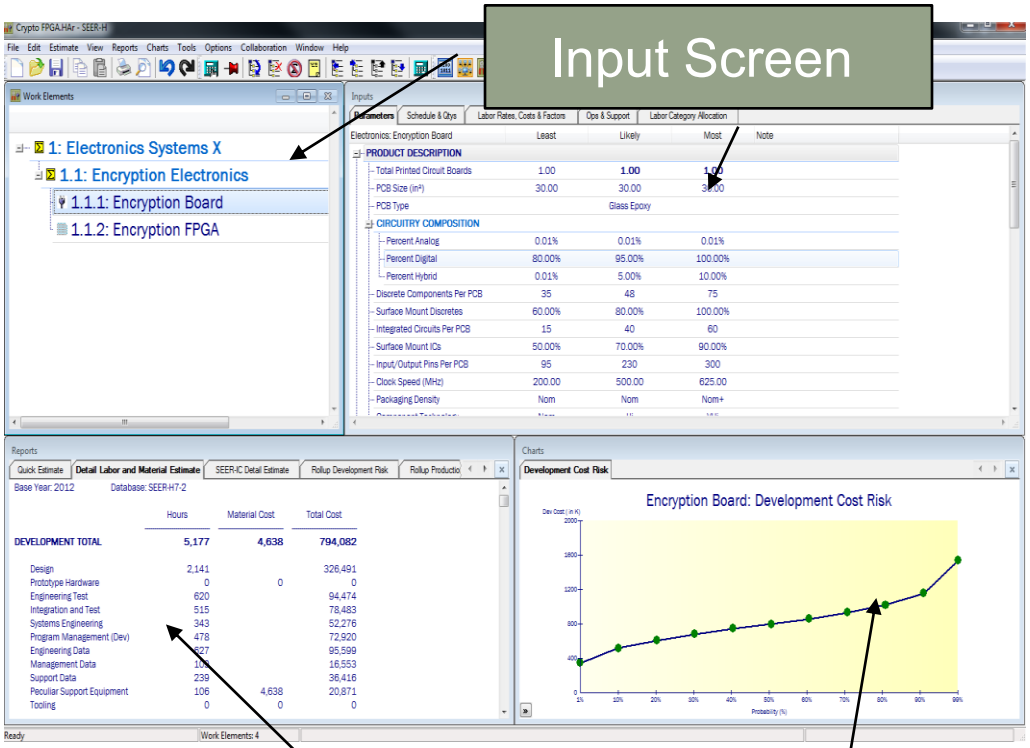
Introduction

- Common parametric models are typically based on some key sizing mechanism (pounds, terminations, SLOC etc)
- However, many costs are incurred in the aerospace industry not only by how "big" a job is, but also by the processes that are required by the customer.
- For this presentation' processes are simply defined as the work products that need to be accomplished on any development
- Key concept: repeatability is the key to predictability

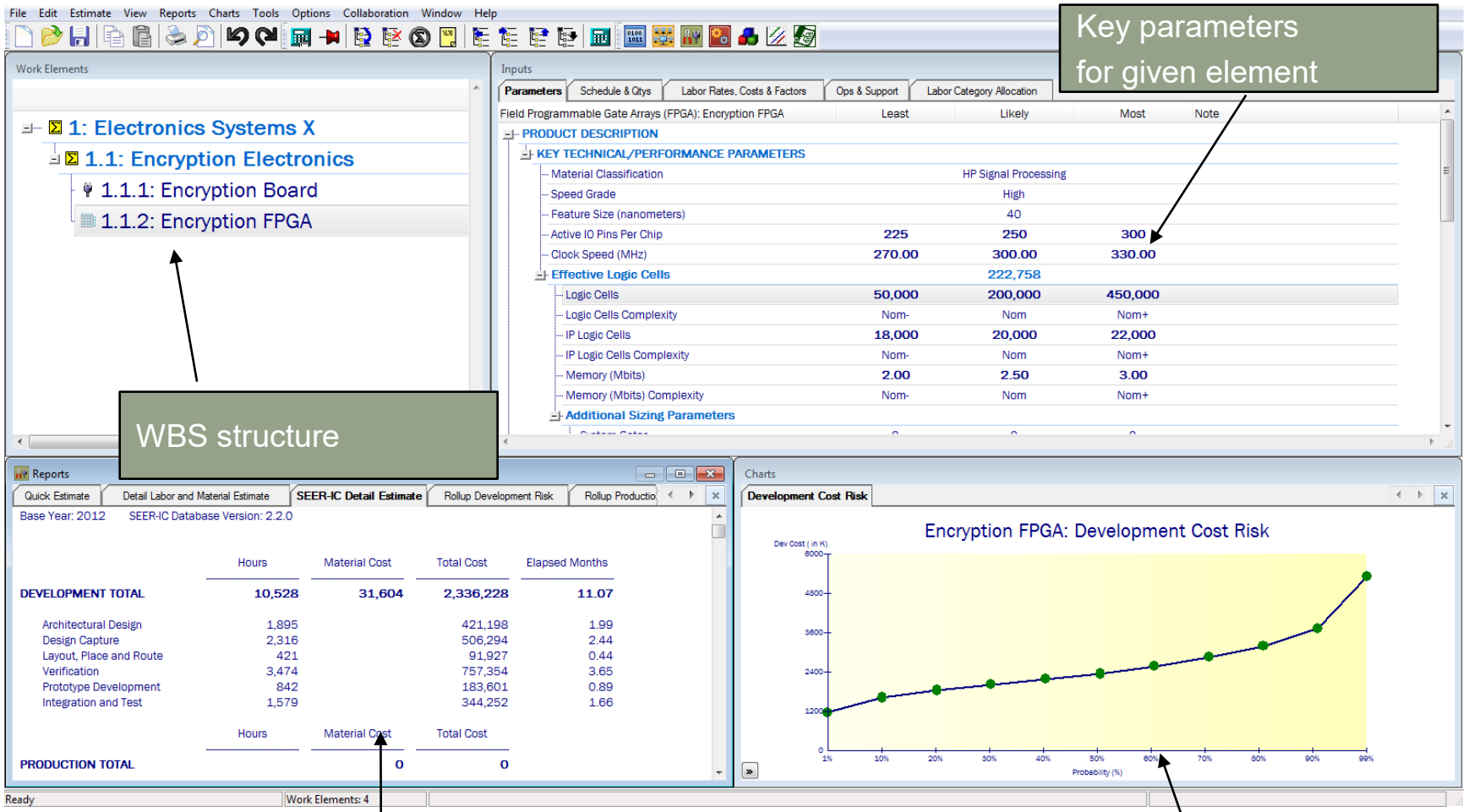


SEER Electronics Example

- Full-tactical Type-1 encryptor
- First product generation
- Base year 2012
- Customer has solid requirements
- 10 Prototypes
- Ground mobile environment
- Development environment has been experiencing some challenges.
- Considerable integration is done at board level.

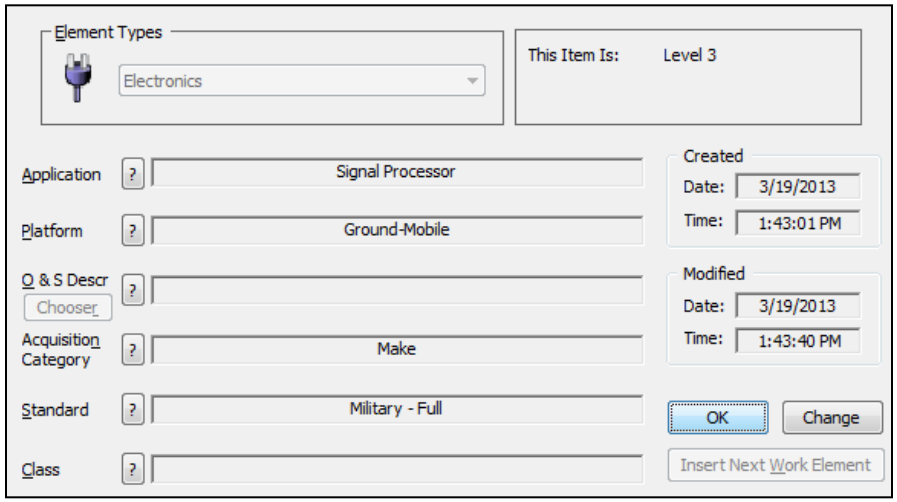


Using SEER to predict FPGA Development Costs



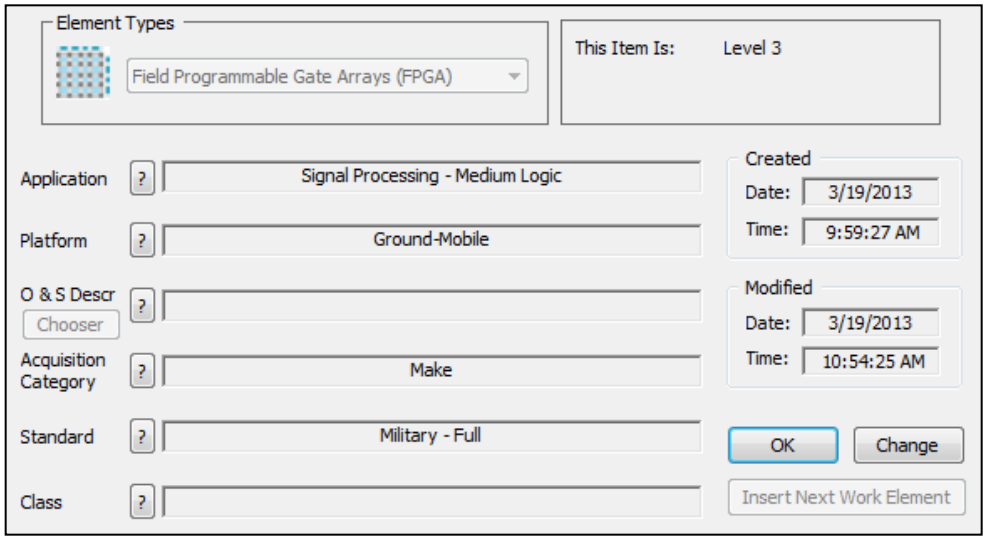
SEER General Element Selections

Board



Knowledge Base Selections

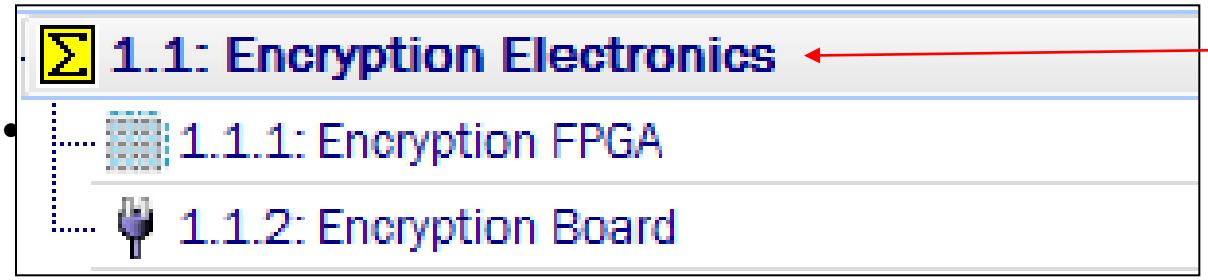
FPGA



These help to set the overall context of the input parameters for a given condition.

SEER Systems Level inputs

These are top level inputs over board and chip



Note yellow rollup indicates Systems activation

SYSTEM LEVEL COST ANALYSIS		YES	
System Engineering and Integration (SEI)		NO	
Integration, Assembly and Test (IAT)		YES	
IAT Development Complexity	Hi-	Hi	Hi+
IAT Development Experience	Nom	Nom	Nom
IAT Production Complexity	Hi-	Hi	Hi+
IAT Production Experience	Nom	Nom	Nom
System Program Management (SPM)		NO	
System Test Operations (STO)		NO	
System Support Equipment (SSE)		NO	

SEER FPGA Inputs

Field Programmable Gate Arrays (FPGA): Encryption FPGA	Least	Likely	Most	Note
PRODUCT DESCRIPTION				
KEY TECHNICAL/PERFORMANCE PARAMETERS				
Material Classification		HP Signal Processing		
Speed Grade		High		
Feature Size (nanometers)		40		
Active IO Pins Per Chip	225	250	300	
Clock Speed (MHz)	270.00	300.00	330.00	
Effective Logic Cells		222,758		
Logic Cells	50,000	200,000	450,000	
Logic Cells Complexity	Nom-	Nom	Nom+	
IP Logic Cells	18,000	20,000	22,000	
IP Logic Cells Complexity	Nom-	Nom	Nom+	
Memory (Mbits)	2.00	2.50	3.00	
Memory (Mbits) Complexity	Nom-	Nom	Nom+	
Additional Sizing Parameters				
System Gates	0	0	0	
Logic Elements	0	0	0	
Multipliers	0	0	0	
Transceivers	0	0	0	
Flip Flops	0	0	0	
DSP Blocks	0	0	0	
Proxy Unit X	0	0	0	
Proxy Unit X Factor	0	0	0	
PROGRAM DESCRIPTION				
New Design	70.00%	80.00%	100.00%	
Design Replication	0.00%	0.00%	0.00%	
Utilization	50.00%	60.00%	70.00%	
Overall Technical Complexity	Nom+	Hi-	Hi	
Complexity - Architecture Design	Nom-	Nom	Nom+	
Complexity - Design Capture	Nom-	Nom	Nom+	
Complexity - Place and Route	Nom-	Nom	Nom+	
Complexity - Verification	Nom-	Nom	Nom+	
Complexity - Prototype Development	Nom-	Nom	Nom+	
Complexity - Integration and Test	Nom-	Nom	Nom+	

Key sizing Inputs. These are done in logic cells.

Note heritage inputs.

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Using SEER to Predict the Cost of Developing the CCA

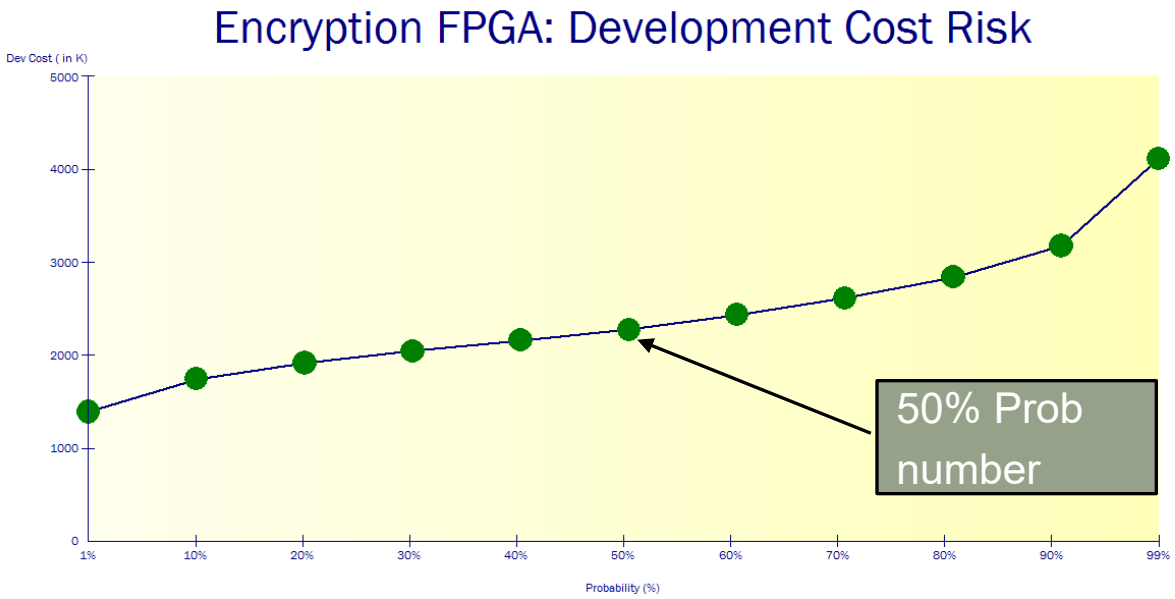
Electronics: Encryption Board	Least	Likely	Most	Note
PRODUCT DESCRIPTION				
Total Printed Circuit Boards	1.00	**1.00**	**1.00**	
PCB Size (in²)	30.00	30.00	30.00	
PCB Type		Glass Epoxy		
CIRCUITRY COMPOSITION				
Percent Analog	0.01%	0.01%	0.01%	
Percent Digital	80.00%	95.00%	100.00%	
Percent Hybrid	0.01%	5.00%	10.00%	
Discrete Components Per PCB	35	48	75	
Surface Mount Discretes	60.00%	80.00%	100.00%	
Integrated Circuits Per PCB	15	40	60	
Surface Mount ICs	50.00%	70.00%	90.00%	
Input/Output Pins Per PCB	95	230	300	
Clock Speed (MHz)	200.00	500.00	625.00	
Packaging Density	Nom	Nom	Nom+	
Component Technology	Nom	Hi	VHi	
Custom Chip Usage		**NO**		
MISSION DESCRIPTION				
Operating Environment		Ground		
Electronics Classification		Computational		
Electronics Fault Detection	0.01%	10.00%	20.00%	
Electronics Fault Isolation	0.01%	5.00%	10.00%	
PROGRAM DESCRIPTION				
New Design	70.00%	80.00%	100.00%	
Design Replication	0.00%	0.00%	0.00%	
Design Complexity	Nom	Nom	Nom	
Certification Level	Low+	Nom-	Nom-	
Subsystem Integration Level	Nom	Nom+	Hi	
DEVELOPMENT ENVIRONMENT				
Developer Capability & Experience	Low+	Nom	Hi	
Development Tools & Practices	Nom	Nom	Nom	
Requirements Volatility	Nom-	Nom	VHi	
Prototype Insertion Method	Nom	Nom	Nom	

SEER Outputs – FPGA

SEER-IC Detail Estimate Report

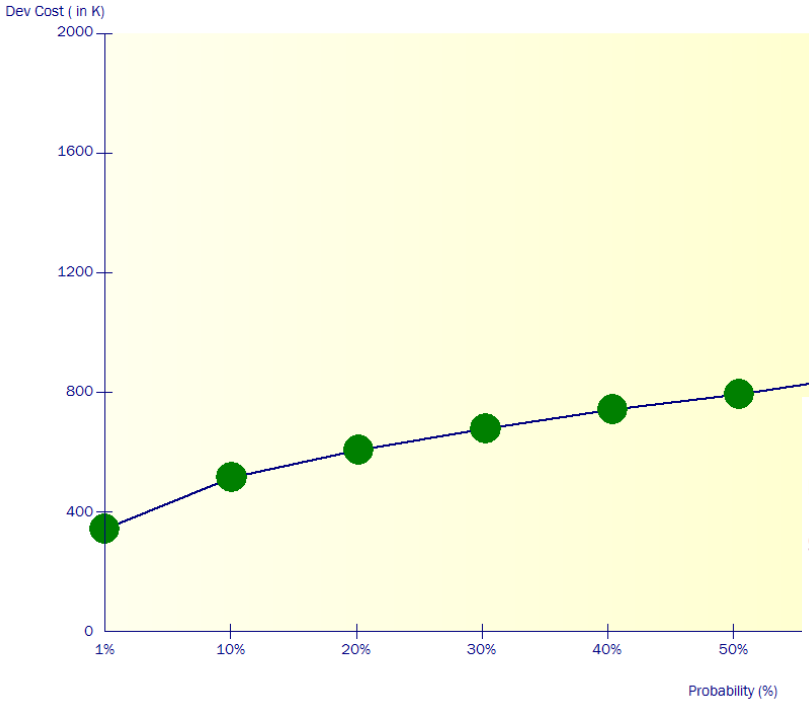
	Hours	Material Cost	Total Cost	Elapsed Months
DEVELOPMENT TOTAL	**10,258**	**28,953**	**2,274,566**	**10.98**
Architectural Design	1,846		410,413	1.98
Design Capture	2,257		493,330	2.42
Layout, Place and Route	410		89,573	0.44
Verification	3,385		737,961	3.62
Prototype Development	821		178,900	0.88
Integration and Test	1,539		335,437	1.65

This report is used to show cost distribution.



SEER Outputs - Board roll up

Encryption Board: Development Cost Risk

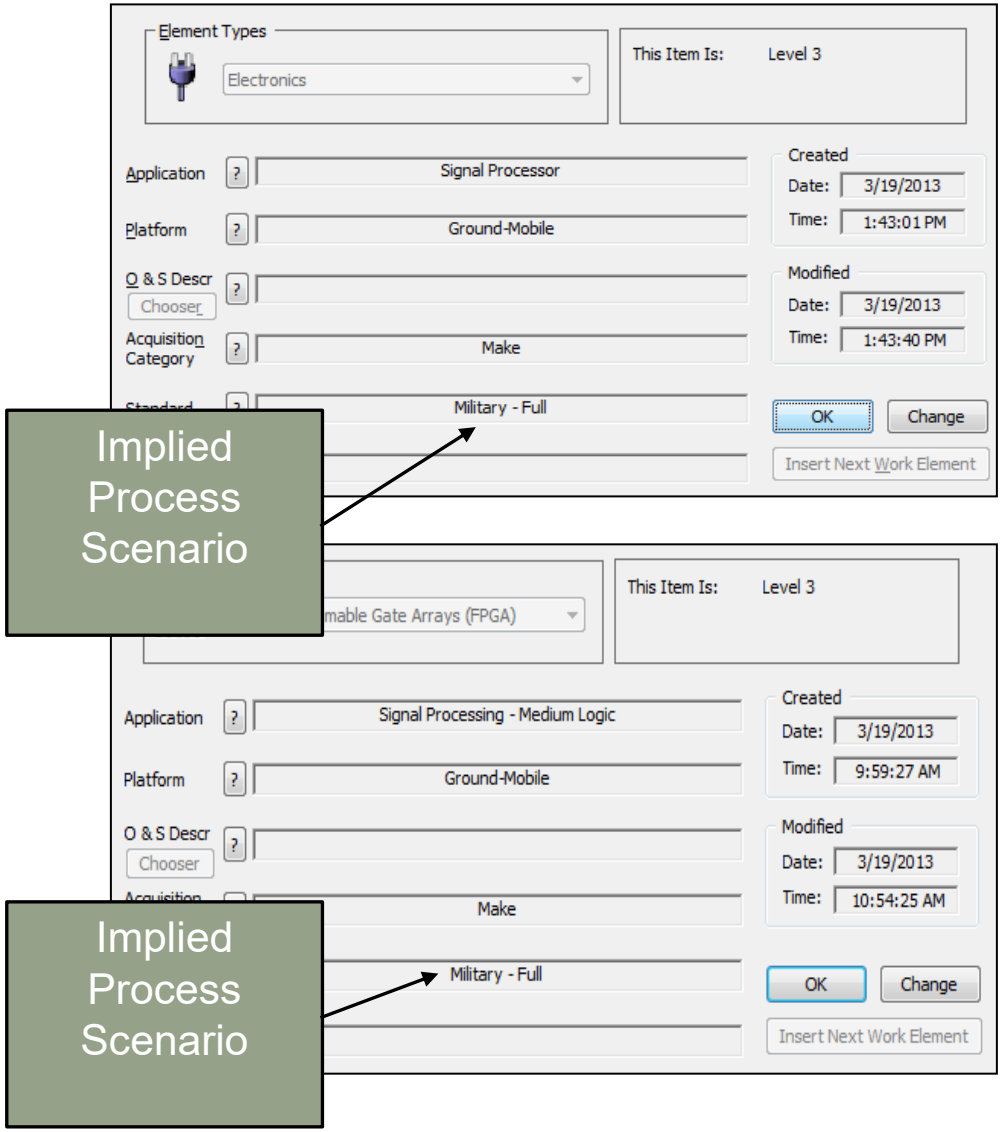


	Hours	Material Cost	Total Cost
DEVELOPMENT TOTAL	**19,001**	**36,242**	**3,635,975**
Subsystem	**15,705**	**36,242**	**3,130,310**
Design	8,688		1,759,737
Prototype Hardware	0	31,604	31,604
Engineering Test	983		174,098
Integration and Test	515		78,483
Systems Engineering	2,343		490,154
Program Management (Dev)	1,568		311,564
Engineering Data	1,096		198,270
Management Data	166		29,113
Support Data	239		36,416
Peculiar Support Equipment	106	4,638	20,871
Tooling	0	0	0
System	**3,296**	**0**	**505,665**
System Engineering and Integration (SEI)	0		0
Integration, Assembly and Test (IAT)	3,296		505,665
System Program Management (SPM)	0		0
System Test Operations (STO)	0	0	0
System Support Equipment (SSE)	0	0	0

Efforts to Integrate chip to board – (complex)

Processes Generally Implied

- Military applications generally require the same type of processes, documentation and review, so lumping all of these into 1 bucket is reasonable
- Generally, most bucket collections revolve around tech demo, tactical and space. There are also subsets for manned space and manned tactical.
- However, the modern customer is now commonly trying to cut costs wherever possible and is willing to accept risk in some cases for tailoring out certain processes in order to reduce costs.



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Capability Maturity Model Integration (CMMI)

- CMMI is a process improvement approach that helps organizations improve their performance. CMMI can be used to guide process improvement across a project, a division, or an entire organization.
- CMMI in software engineering and organizational development is a process improvement approach that provides organizations with the essential elements for effective process improvement.
- CMMI is a trademark owned by Software Engineering Institute of Carnegie Mellon University.
- According to the Software Engineering Institute (SEI, 2008), CMMI helps "integrate traditionally separate organizational functions, set process improvement goals and priorities, provide guidance for quality processes, and provide a point of reference for appraising current processes."

- Maturity Levels
  - There are Five maturity levels. However, maturity level ratings are awarded for levels 2 through 5.
- Maturity Level 2 - Managed
  - CM - Configuration Management
  - MA - Measurement and Analysis
  - PMC - Project Monitoring and Control
  - PP - Project Planning
  - PPQA - Process and Product Quality Assurance
  - REQM - Requirements Management
  - SAM - Supplier Agreement Management
- Maturity Level 3 - Defined
  - DAR - Decision Analysis and Resolution
  - IPM - Integrated Project Management +IPPD
  - OPD - Organizational Process Definition +IPPD
  - OPF - Organizational Process Focus
  - OT - Organizational Training
  - PI - Product Integration
  - RD - Requirements Development
  - RSKM - Risk Management
  - TS - Technical Solution
  - VAL - Validation
  - VER - Verification
- Maturity Level 4 - Quantitatively Managed
  - QPM - Quantitative Project Management
  - OPP - Organizational Process Performance
- Maturity Level 5 - Optimizing
  - CAR - Causal Analysis and Resolution
  - OPM – Organizational Performance Management

Levels 4 and 5 commonly referred to as "High Maturity" maturity

http://en.wikipedia.org/wiki/CMMI

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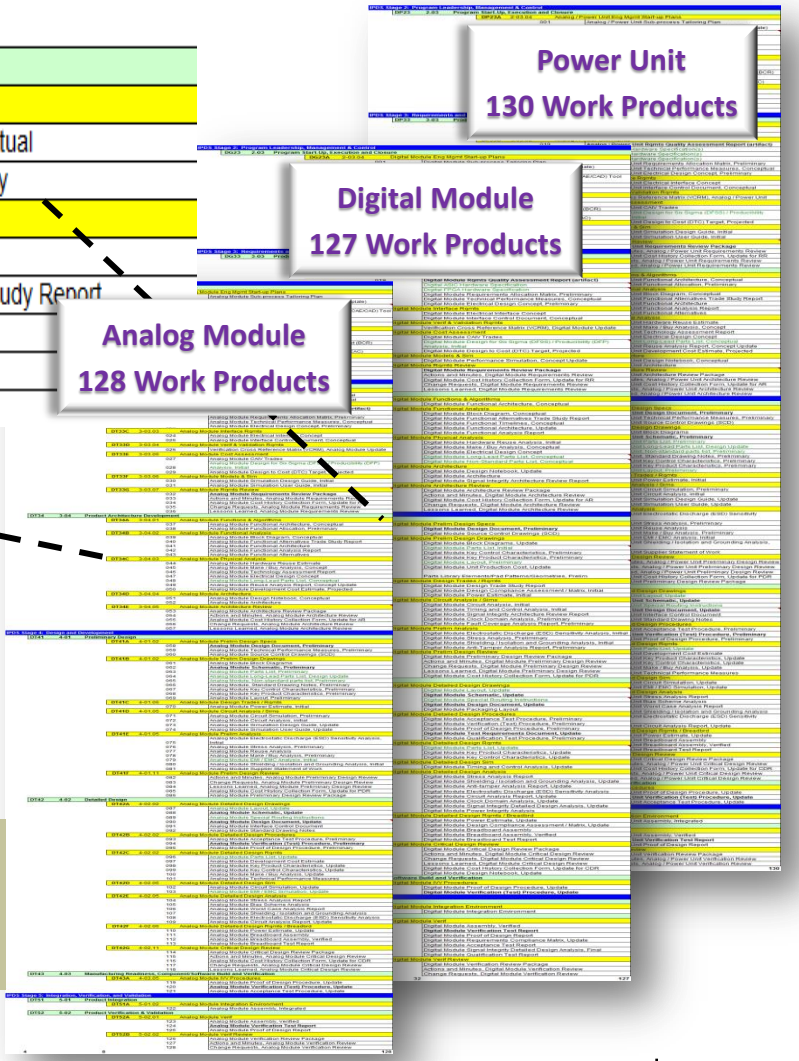
Introduction to Process Based Product Development

At Level 3, an organization ….	At level 4 (High Maturity), an organization additionally…
… defined work products … ordered work products … these are processes … complies to its process standards … makes process improvements … contributes lessons learned … captures and reacts to measures … performs corrective action	… uses measures to *predict* performance and take *proactive* corrective actions … achieves its expected outcome through changes required by a *predicted outcome* **And for Level 5:** … looks to *eliminate* special cause and common cause *variation* … drives for incremental and innovative process improvements based on its *quantified goals*

Predictability ⇨ Achieving Business Goals

What Do Work Products Look Like?

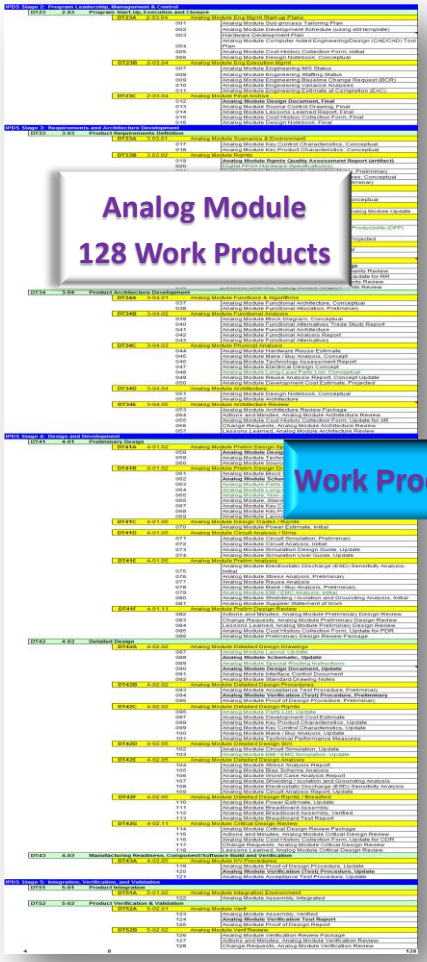
DT34	3-04	Product Architecture Development	
	DT34A	3-04.01	Analog Module Functions & Algorithms
		037	Analog Module Functional Architecture, Conceptual
		038	Analog Module Functional Allocation, Preliminary
	DT34B	3-04.02	Analog Module Functional Analysis
		039	Analog Module Block Diagram, Conceptual
		040	Analog Module Functional Alternatives Trade Study Report
		041	Analog Module Functional Architecture
		042	Analog Module Functional Analysis Report
		043	Analog Module Functional Alternatives



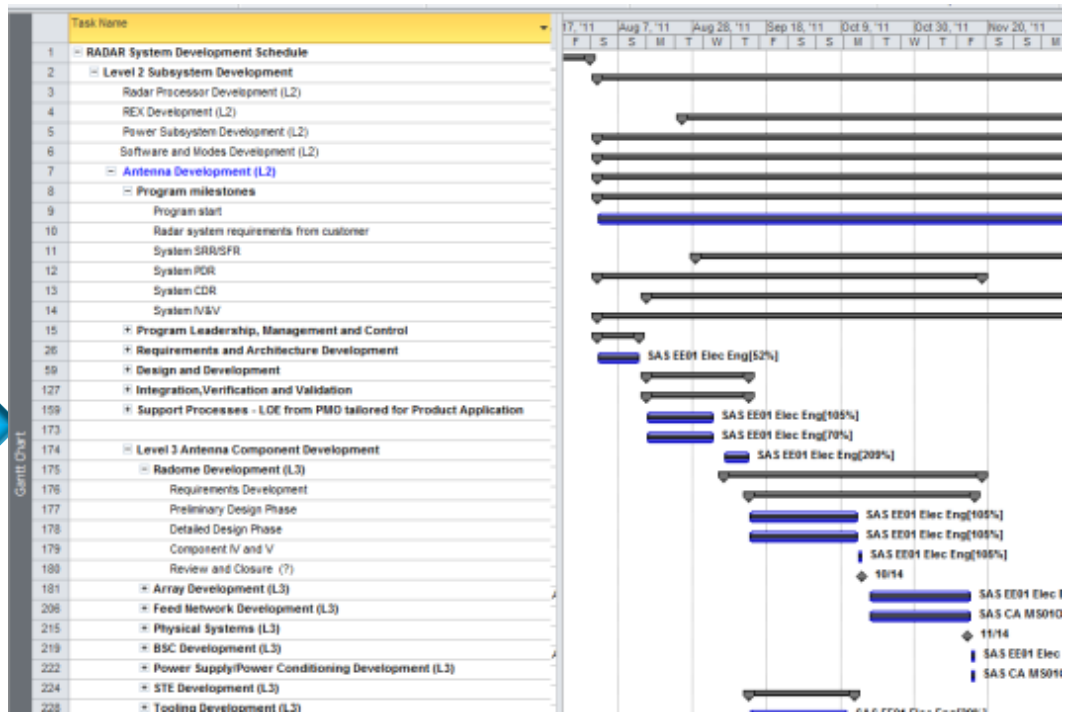
I'm sorry……did you say 130 work products

Moving from adhoc to defined work products

Turn Work Products into Scheduled Tasks



Work Products Become Tasks



The problem is that tracking 130 TTDs is too much

Creating an Achievable Execution Plan

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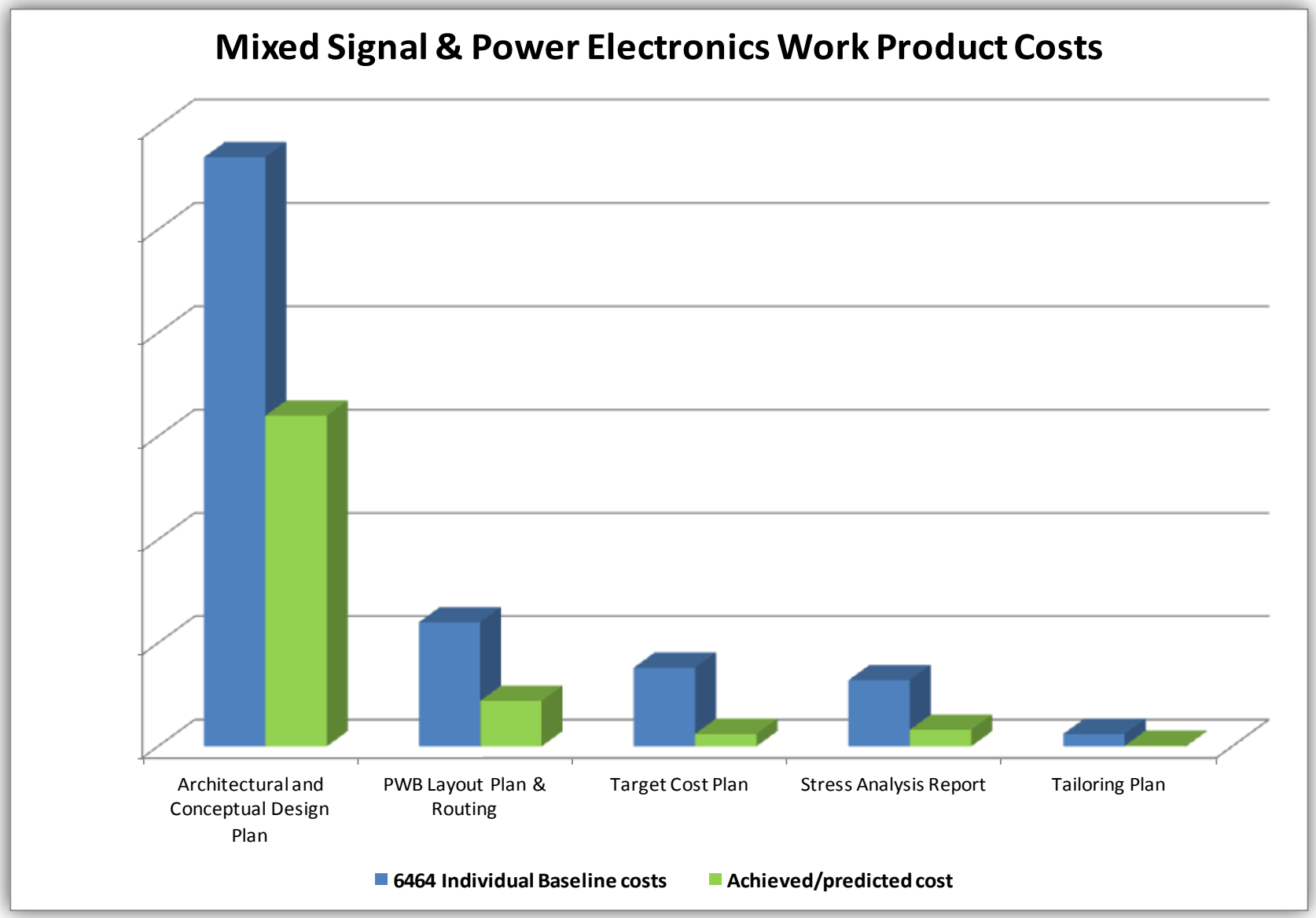
Tracking Developing Costs in a List

- Notice that the design process now becomes a repeatable process
- Repeatable is the key to predictable
- Further, for things that are repeated, examples and templates can be developed for increasing the amount of reuse
- In terms of analysis, each of the tasks in the phases can now be evaluated for productivity improvement when enablers come on board

Phase	Set of Tasks	Notional Hours
Start-up	Tailoring Plan	40
	Project Management Plan	40
	Hardware Development Plan	40
	Architectural & Concept. Design Plan	40
Requirements and Architecture	Target Cost Plan	40
	Product Specification	40
	Interface Control Document	40
	Simulation & Analysis Report	40
	Requirements & Architectural Review Package	40
Preliminary Design	Supplier Statement of Work	40
	Parts List / Plan	40
	Grounding & Shielding Drawing	40
	Schematic	40
	Stress Analysis Report	40
	Power Dissipation & Analysis Report	40
	Source Control Drawing	40
Detailed Design	PWB Layout Plan & Routing	40
	Test Procedure	40
	CDR Package	40
IV&V	Integration & Test Report	40
	Verification Review Package	40

Improved Productivity and Predictivity



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Conclusion

- Key concept is repeatability is the key to predictability
- The ability to break down a development effort in terms of repeatable processes (work products) is beneficial for the cost estimation process
- Attacking each of the process areas is how to fundamentally improve costs

Backup and Bio slides

David Bloom Bio

Biography:

After graduating from the University of California at Davis in 1983, Mr. Bloom has worked for the Naval Weapons Center, Lockheed Martin, Lawrence Livermore National Labs and since 2008, for Raytheon Space and Airborne Systems (SAS) where he is a Sr. Engineering Manager.

Mr. Bloom is currently the Cost Estimation Subject Matter Expert (SME) for the Electronics Center of SAS. He has developed parametric models for all Electronics Center products and helped transform the culture of the organization in the use of parametric bidding methodologies.

In addition to Mr. Bloom's focus for the Electronics Center in developing parametric cost models for the design and development cycle activity of electronics sub-products, he is also leading the effort to reduce the cost of FPGA and ASIC development by modernizing the Digital Verification methods and establishing reproducible re-use methods.

Mr. Bloom has 2 patents and a software copyright along with a number of publications ranging from electromagnetic boundary value problems to cost estimation. In 2006, he won the International R&D 100 Award for innovating a cost effective Gigapixel Camera for persistent surveillance applications.

Chris Fudge Bio

Biography:

Chris Fudge has been in the Aerospace & Defense Electronics business for over 30 years. He began his career at Hughes Aircraft Electro-Optical Systems in Manufacturing and transitioned to engineering in 1991. Chris was divested to DRS Sensors and Targeting Systems in 1998 where he held positions of Chief Engineer, Program Manager and Deputy VP of Engineering. Upon his return to Raytheon in 2005, Chris has held positions as lead Systems Engineer, Chief Engineer and is currently the Department Manager of the Mixed Signal & Power Products organization. In addition to his management background, Chris has designed electronic circuit cards and FPGA's for a host of military platforms including the M1A2 tank, Bradley Fighting Vehicle and the Apache helicopter. Chris holds a Bachelors of Science degree in Electrical Engineering from Long Beach State University.

