# Challenges in Estimating the Development Cost of Microcircuit Technology

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# Introduction

- Electronics Technology progresses at an incredible pace!
- Completes an entire life cycle every 3-5 years (on average)
- Thanks to today's technologies, the functionality that used to take an entire Circuit Card Assembly can now be integrated into a single chip
  - 'System-on-a-Chip'
- This has revolutionized not only the technology, but also the design processes and tools used to design these solutions
- CAE and CAD tools are now integrated, consequently the roles of Electrical, Mechanical Engineers and Designers have changed
- All of this leads to major challenges in estimating the cost for new electronics / microcircuit costs
- This paper looks at some of the more recent changes in microcircuit technology, and discusses some ideas on how best to estimate these costs

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# Moore's Law

Moore's Law Video

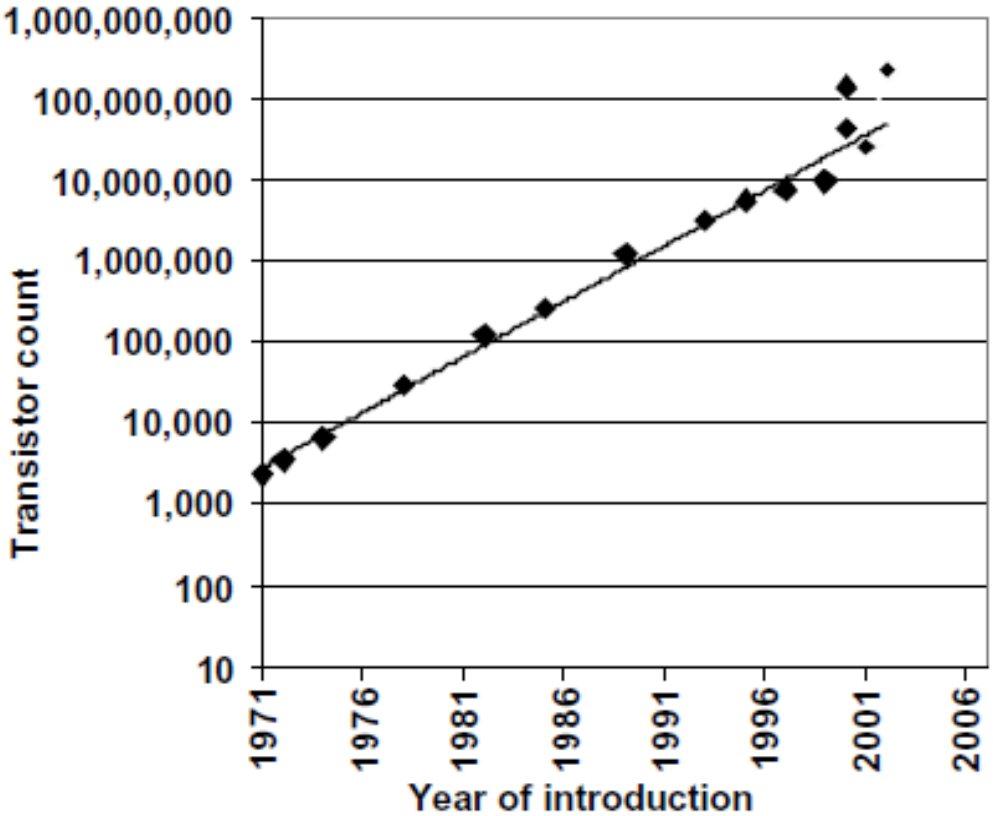


Figure 1 – Transistor count doubles every 18-24 months [5, 6]

From Mainframes to Desktop PCs to Notebook PCs to Tablets to Smartphones to Smart Watches, to Smart Cars, electronics technology is advancing at incredible rates

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# Memory

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# Memory Cost Estimation

- Development cost not an issue since these are commodity items
- Still a desire for the cost analyst to be able to estimate recurring cost (include in a larger cost model), without taking the time to research costs
- Many types of Memory available in todays market
  - RAM (SRAM, PRAM, RRAM, MRAM), Flash, EEPROM, (EPROM, PROM – less used)
- Generally characterized by Type, Size (Bytes), Data Rate (Speed), and Design Rules
  - Good Cost Drivers
- Memory technology / types progressing at amazing pace
  - Requires dedicated cost research resources to keep models up to date
  - Updates at least every couple of years

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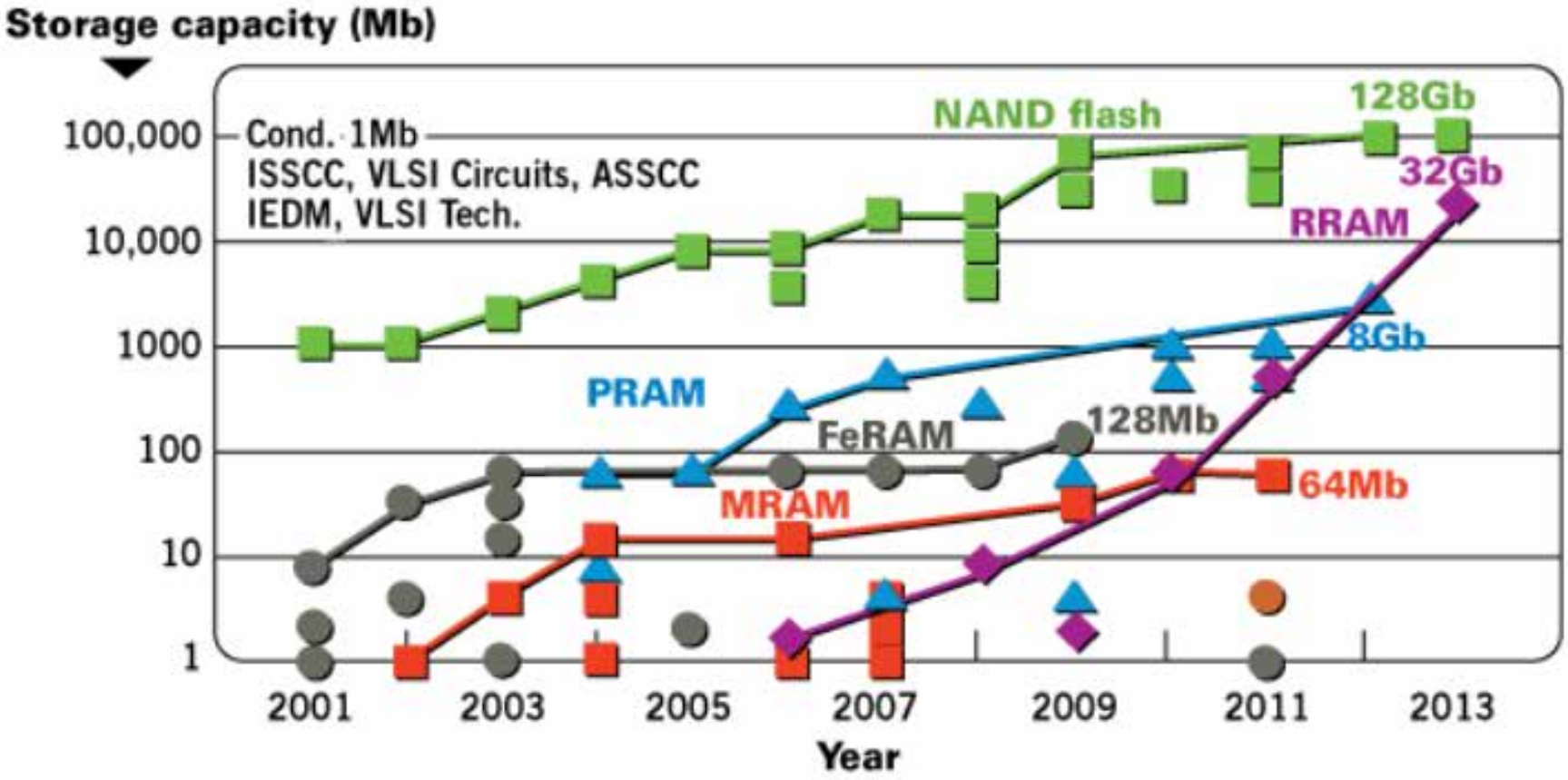
# Memory Storage Capacity over Time




Memory storage capacity has increased by 10x every 6 years on average

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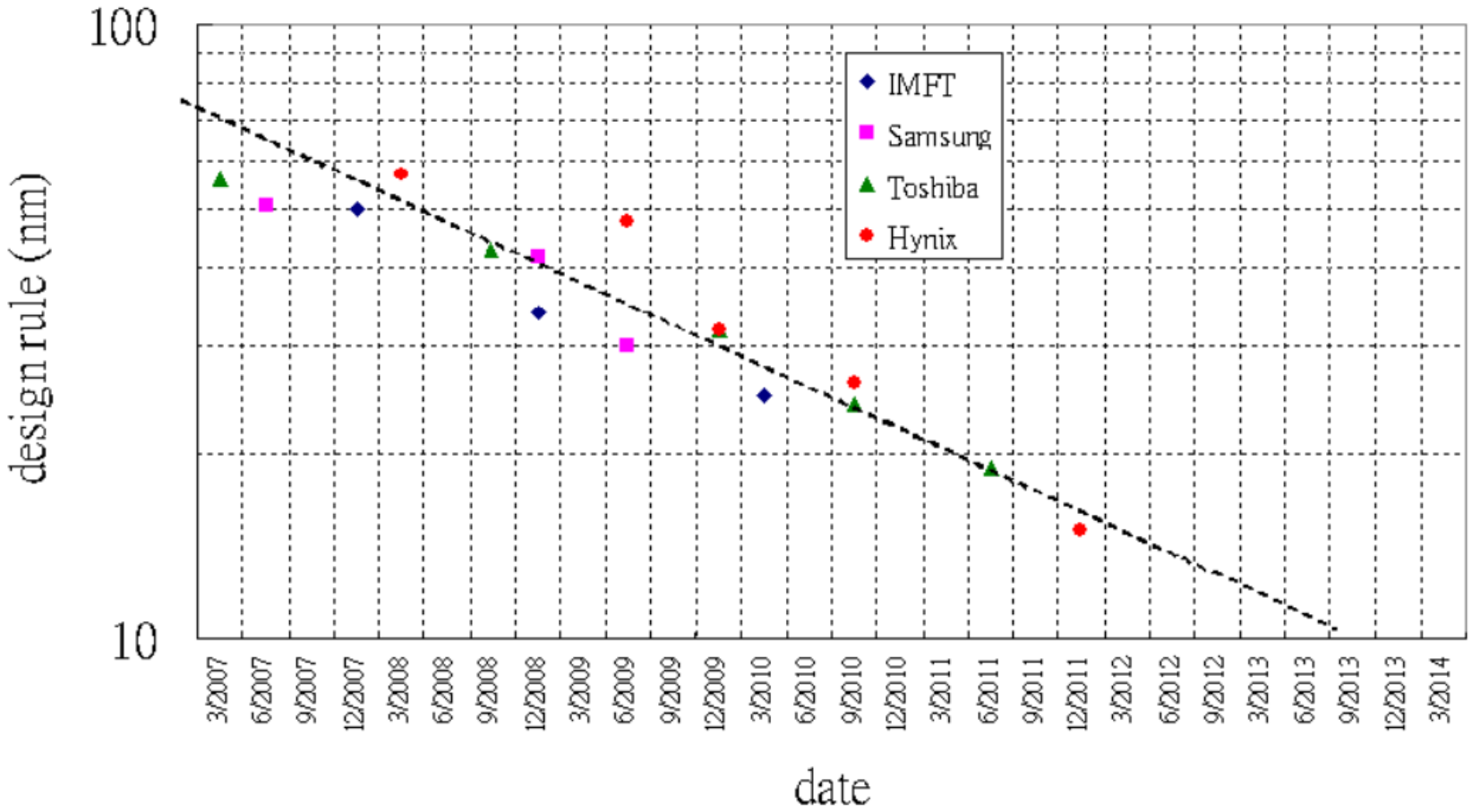
# Design Rule (Lithography) Change over Time




Design Rule (Lithography) feature size has decreased by 2X every 2 years on average

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# Microprocessors

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# Microprocessor Cost Estimation

- Similar to Memory, development cost is not too much of an issue at the part level
- Main element of development cost associated with microprocessors is the design / interface with the associated supporting 'chip-sets'
  - Module / CCA level development cost
  - Somewhat related to microprocessor pin counts
  - Supported by manufacturer Board Support Packages / Development Kits, which significantly reduce module / CCA level design efforts
- Still a desire for the cost analyst to be able to estimate recurring cost (include in a larger cost model), without taking the time to research costs
- Primary production cost drivers are Lithography (feature size) and Transistor Count
- Fast moving technology that requires frequent cost model maintenance

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# Monolithic Microwave Integrated Circuits (MMIC's)

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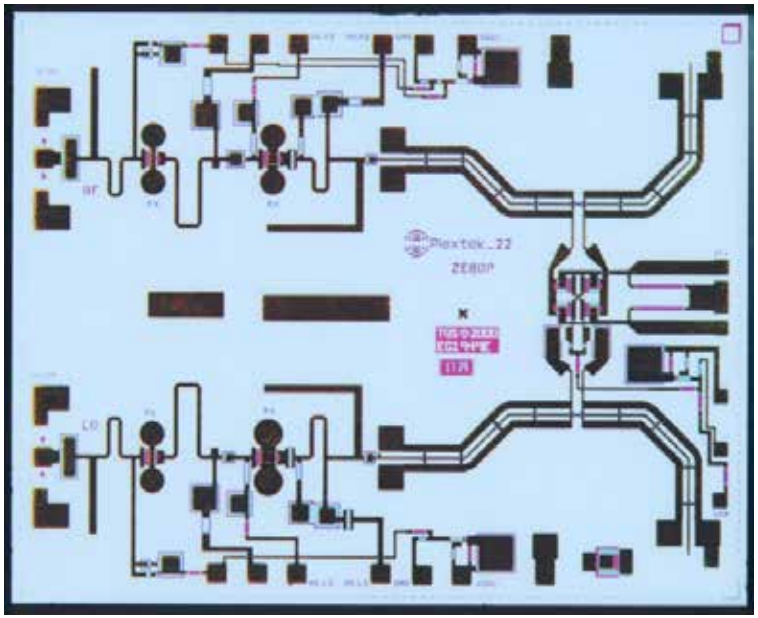
# MMIC's

- A Monolithic Microwave Integrated Circuit (MMIC) is a totally integrated microwave circuit on one chip
- Distributed elements are included along with active (FETs, diodes) and other passive elements (capacitors, resistors)
- Typical substrate materials include GaAs, SiGe HBT, and GaN
  - Materials that provide high transistor $f_t$ (cut-off frequency)
  - SiGe for EHF low noise figure applications
  - GaN can provide more RF power and better efficiency for state-of-the-art Microwave Transmitter applications



**Legend:**
GaAs: Gallium Arsenide
SiGe: Silicon Geranium Heterojunction Bipolar Transistor
GaN: Gallium Nitride

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# Estimating the Cost of MMIC's

- Initial Research and Development (R&D) in the development of Active and Passive elements for a new substrate, which then becomes a component library for reuse
- NonRecurring Engineering (NRE) for developing application specific microwave circuits, including the routing and placement of active and passive elements along with distributed elements to perform an application specific function
- Cost Drivers include:
  - Number of iterations needed to obtain desired performance (Wafer runs)
  - Computer Aided Engineering (CAE) / Computer Aided Design (CAD) process / tools used
  - Testing costs (On-wafer continuity and chip probing, and packaged part functional testing)

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# Field Programmable Gate Array's (FPGA's)

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# Field Programmable Gate Arrays (FPGA's)

- FPGA: Integrated Circuit programmed after manufacture by the user
  - Provides application specific functions (initially custom logic on one chip, but today, almost any complex digital functionality you can imagine)
- Basic FPGA contains arrays of programmable logic blocks, e.g. AND, XOR gates, and RAM blocks
  - Complex digital computation capability
- Modern FPGAs also include microprocessors
  - 'System-on-a-chip'
- Some modern FPGAs feature programmability at run time
- Programmed with the VHDL (VHSIC Hardware Description Language) programming language
  - Most similar to ADA, with some C++ features
  - Newer custom languages also being used

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# State-of-the-art FPGA and VHDL Code Sample

## Altera EP4SGX230K FPGA

- 40 nm
- 91,200 ALMs
- 228,000 LEs
- 182,400 Registers
- 1,235 M9K & 22 M144K memory blocks
- 14,283 Kb embedded memory
- 1,152 pin FGBA, 35mm Sq, 1.0 mm pitch

## VHDL Sample

```
1 library ieee;
2 use ieee.std_logic_1164.all;
3 use ieee.numeric_std.all;
4
5 entity signed_adder is
6   port
7   (
8     aclr : in    std_logic;
9     clk  : in    std_logic;
10    a    : in    std_logic_vector;
11    b    : in    std_logic_vector;
12    q    : out   std_logic_vector
13  );
14 end signed_adder;
15
16 architecture signed_adder_arch of signed_adder is
17   signal q_s : signed(a'high+1 downto 0); -- extra bit wide
18
19 begin -- architecture
20   assert (a'length >= b'length)
21     report "Port A must be the longer vector if different sizes!"
22     severity FAILURE;
23   q <= std_logic_vector(q_s);
24
25   adding_proc:
26   process (aclr, clk)
27     begin
28       if (aclr = '1') then
29         q_s <= (others => '0');
30       elsif rising_edge(clk) then
31         q_s <= ('0'&signed(a)) + ('0'&signed(b));
32       end if; -- clk'd
33     end process;
34
35 end signed adder arch;
```

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# Estimating the cost of FPGA's

- So, the primary development cost of an FPGA is not the chip itself, or even the CCA it is mounted to, but the cost of programming the chip
- The challenge then becomes how to best estimate the cost of programming the chip
- Key Cost Drivers:
  - Size (Firmware lines of code or FPGA capacity in terms of Active Look Up Tables, Configurable Logic Block Flip Flops and System Logic Cells)
  - Code Complexity and Implementation & Verification Complexity
- Two major steps:
  - Generating the firmware code to define the functionality: typically VHDL
  - Compiling the code to generate the logic programmed on the chip
- The VHDL cost can be estimated similar to other software
- The Implementation & Verification can be refined based on complexity factors associated with things like timing, memory, and performance

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# FPGA Cost Estimation Challenges

- What is the best sizing metric?
- Software Size (SLOC, Function Points, others)
  - Pros:
    - *Known early in the development cycle*
    - *Hardware Independent*
    - *Much research exists into appropriately measuring and using software size as a cost driver*
  - Cons:
    - *Does not appropriately "size" issues that arise late in the development cycle*
    - *Not the sizing metric of choice for FPGA developers*
- Active Logic Cells
  - Pros:
    - *Common sizing metric used by FPGA developers*
    - *Changes to reflect implementation issues arising late in the design cycle*
  - Cons:
    - *Can only be measured later in the development cycle.*
    - *Definition changes depending on vendor, and even FPGA models by the same vendor*
    - *ALC counts depend on the model of FPGA and synthesis software.*

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# FPGA Cost Estimation Challenges

- Implementation Complexity difficult to quantify
- Possible contributors to implementation complexity include:
  - Communication/Timing Constraints
  - Memory Constraints
  - Performance Constraints
- Constraints depend on
  - The application (i.e. real-time signal processing often has significant constraints)
  - The FPGA specs (Some come with more logic cells, or more memory, etc. Can have different FPGA architectures that have may be better or worse at meeting performance or timing constraints)
  - Design growth (FPGAs are reprogrammable, but if the design grows too much, can hit significant constraints for later revisions, requiring upgrading to a different model)

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# Microcircuit IP Cost Estimation Challenges

- Custom ICs are commonly based on a mix of new and reused designs/intellectual property (IP)
- With respect to Microcircuits IP is knowledge of existing design, e.g. HDL code, previously synthesized logic
- Reusing IP is not free!
  - It is usually necessary to modify the design to implement new features, optimize the design, or interface with other logic blocks.
- Approximate effort to incorporate reused IP compared to new*
  - Specification and Design: ~40%
  - Detailed Design and Development: ~40%
  - Verification and Testing: ~30%
  - Also include new costs (search, evaluation and selection of IP, licensing cost for 3rd party IP)

* From A. Dey and J. Moudy. Cost Savings via Reuse

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# Summary

- Microcircuit technology is constantly evolving, at a rapid pace
- Not only are the components increasing in size and complexity per unit area, design methods and tools are evolving as well
- Makes microcircuit cost estimation a challenge
- Cost models need to be constantly updated to keep pace with technology
- Requires dedication in both cost research as well as model / product development

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# Additional Reference

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# What is a Microcircuit?

## microcircuit

### English [edit]

**Etymology** [edit]

*micro- + circuit*

Wikipedia has an article on: **microcircuit**

**Noun** [edit]

**microcircuit** (*plural* **microcircuits**)

1. An electronic device, usually fabricated by photolithography, that is very small and implements several components or their equivalent; an integrated circuit.

Categories: English words prefixed with micro- | English lemmas | English nouns | English countable nouns

- Includes:
  - Electronic modules
  - Printed Circuit Boards (PCBs)
  - Multi-Chip Modules (MCMs)
  - Application Specific Integrated Circuits (ASICs)
  - Field Programmable Gate Arrays (FPGAs)
  - Fully custom-developed microcircuit chips
  - Other components
    - *Purchased components, e.g. IC's, capacitors, resistors, inductors, etc.*

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# Memory Example: Micron 512Gb NAND Flash

- 512 Gb
- 333 MT/s

- ~16 nm lithography

- Package Size: 18 mm x 14 mm
- Package: LBGA
- 152 ball (pins)

- $77

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# Processor Example: Intel Core i7-6700

- 64 bit
- 4 Cores
- 8M Cache memory
- 4.0 GHz clock speed
- 14 nm lithography
- Package Size: 37.5 mm x 37.5 mm (Die Size: ~27.5 mm x 27.5 mm)
- Package: Flip Chip Land Grid Array
- 1151 pins
- $312

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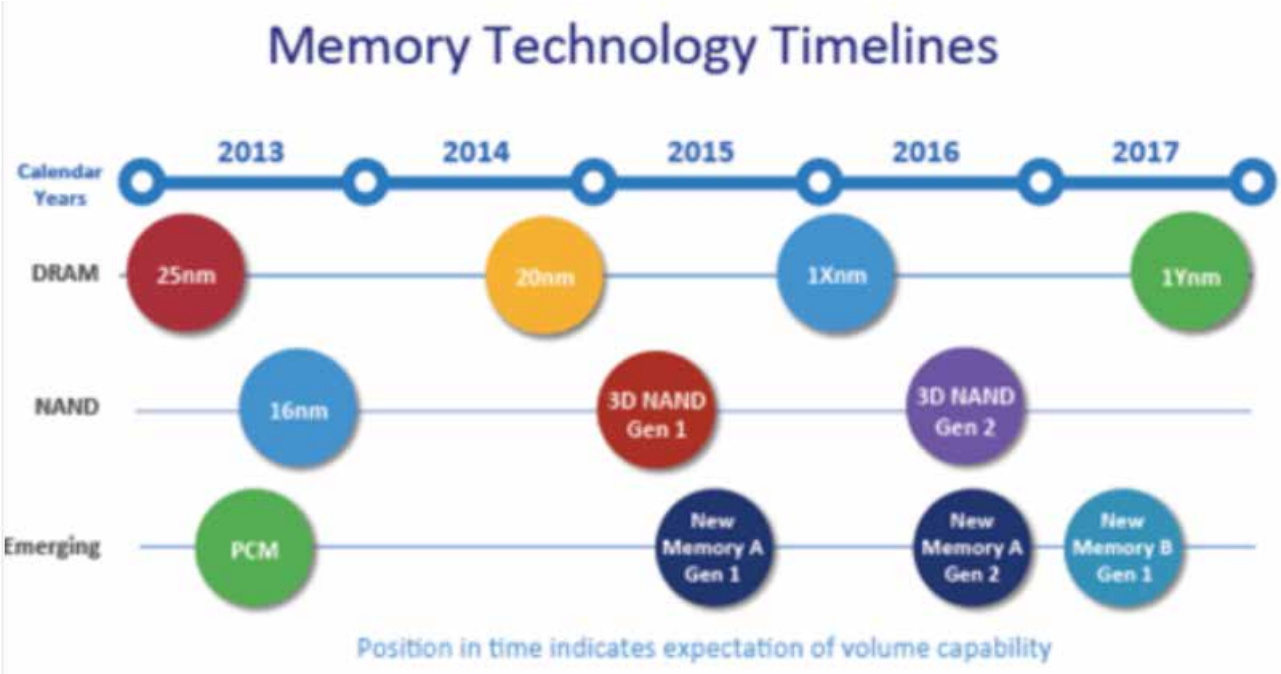
# Memory Timelines

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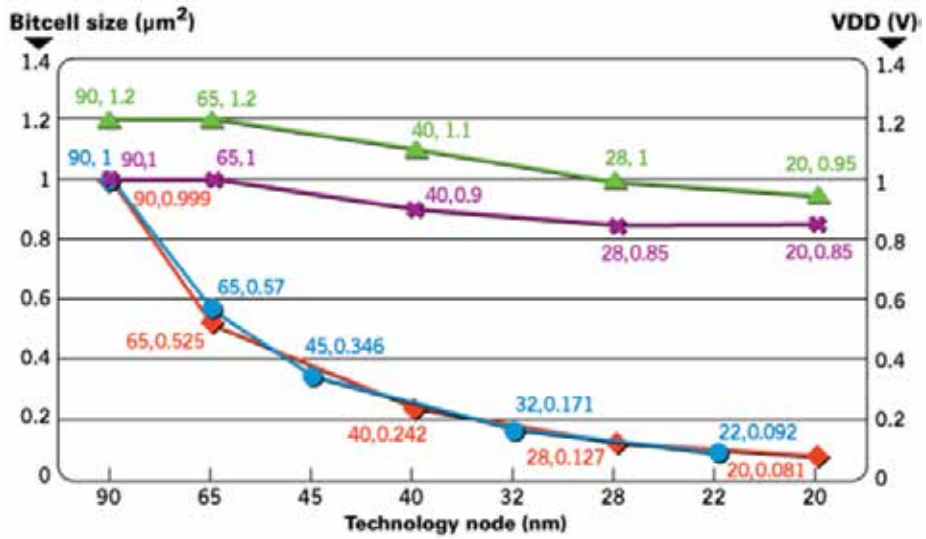
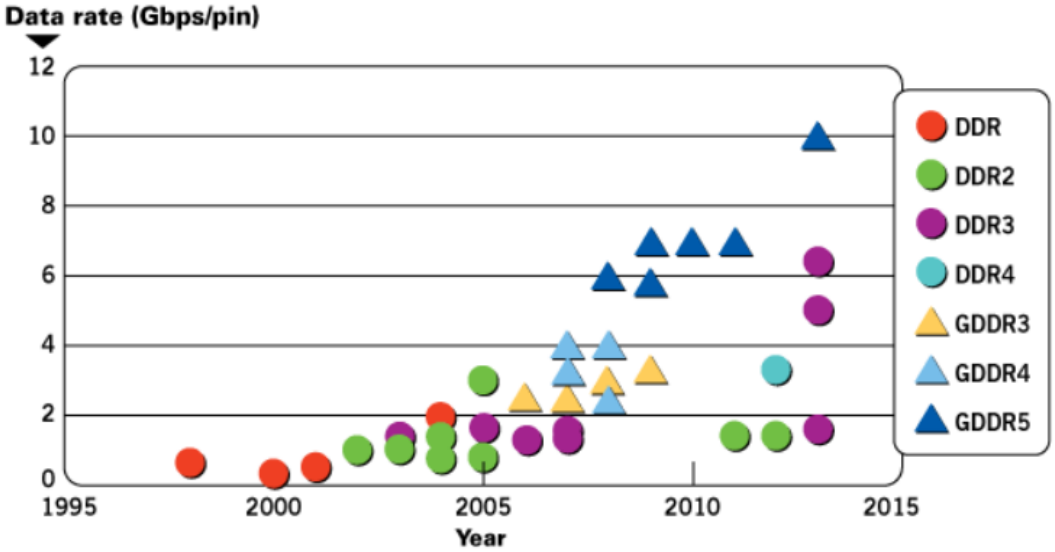
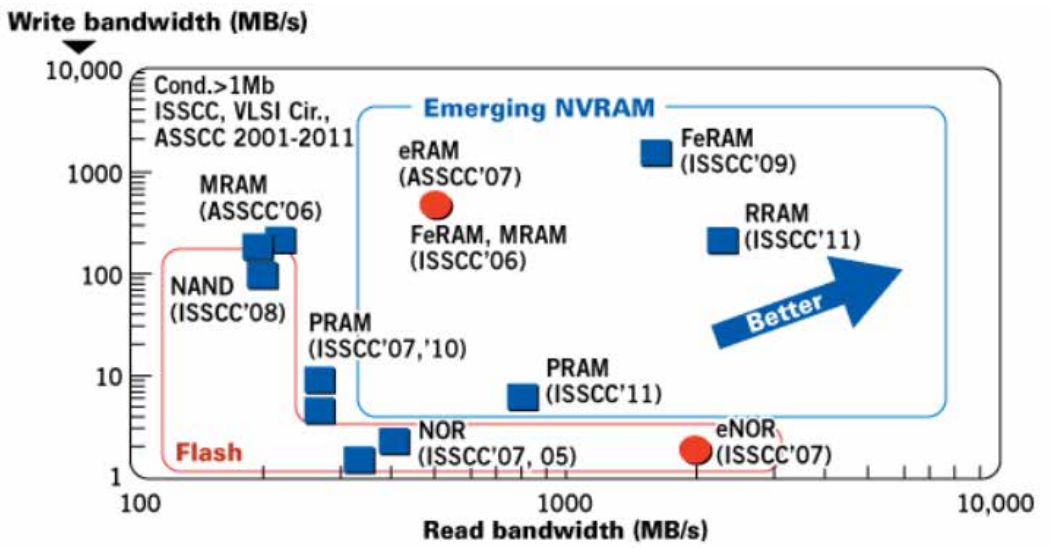
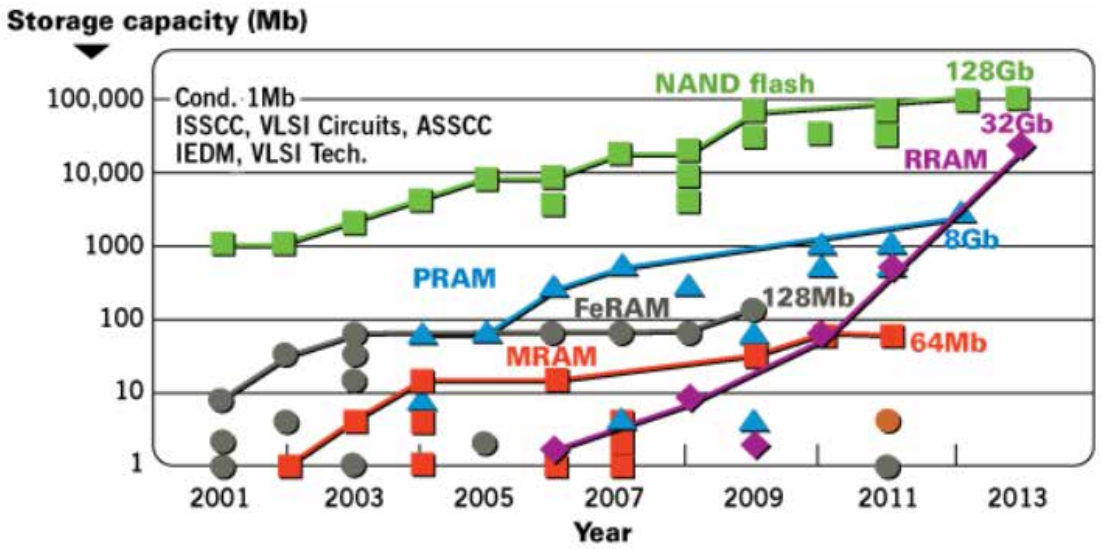
# Memory Trends (cont.)



# Memory Trends (cont.)

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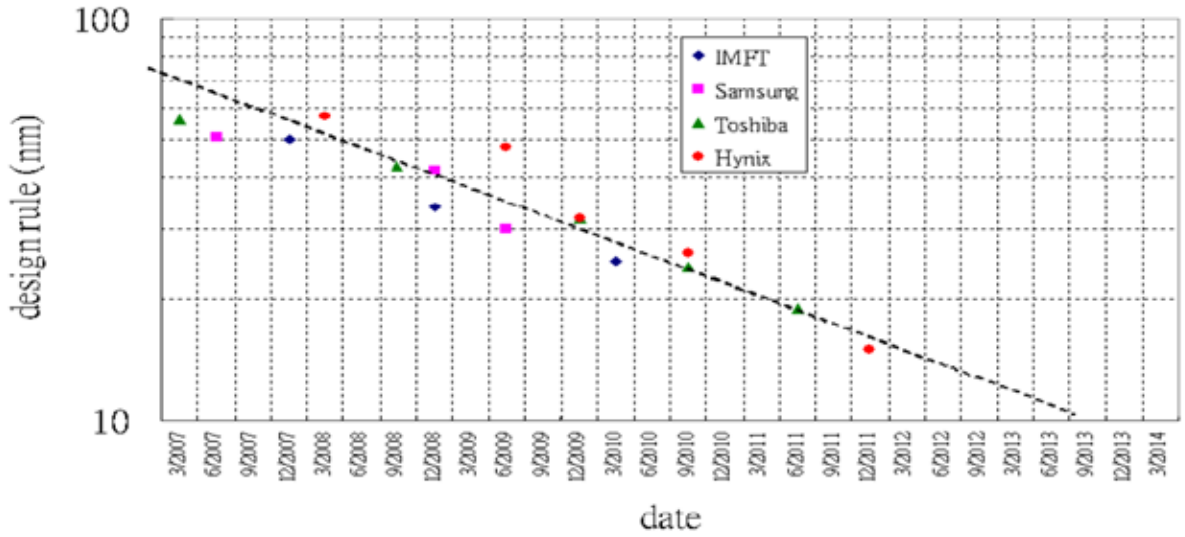
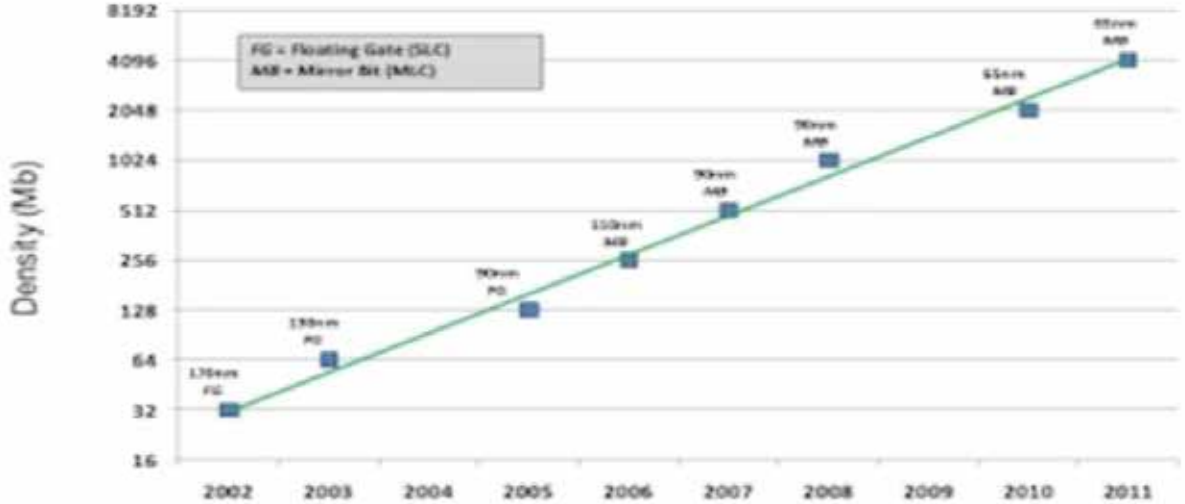
# Memory Trends (cont.)




* A higher density node was not released in 2004 and 2009.

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# Processor Timelines

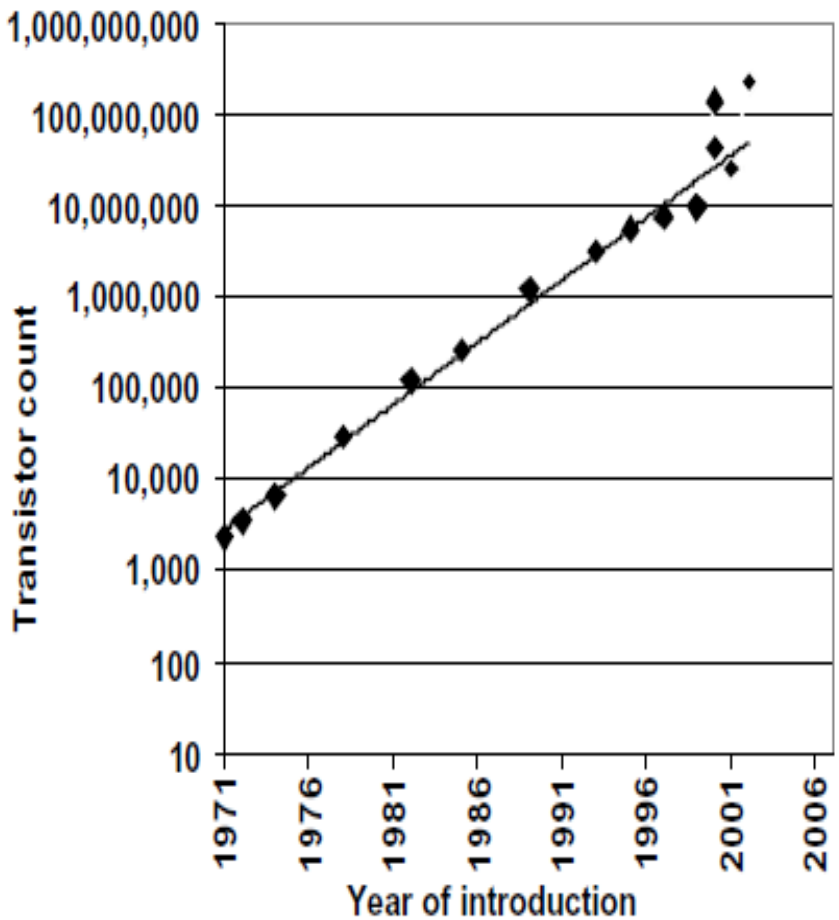


Figure 1 – Transistor count doubles every 18-24 months [5, 6]

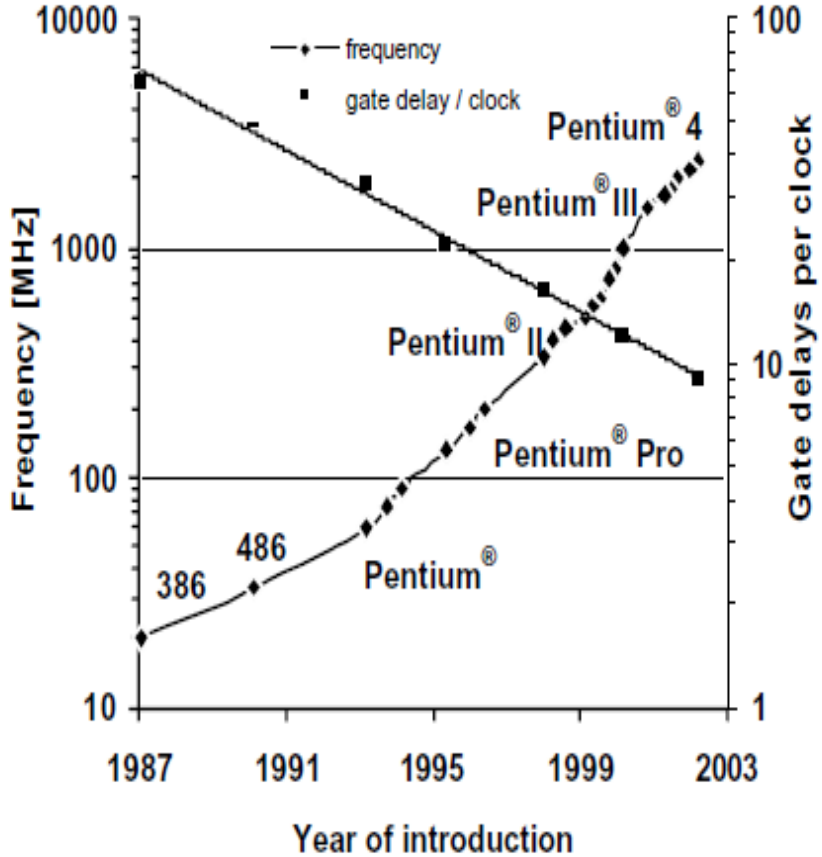


Figure 2 – Frequency doubles and number of gates per clock reduced by 25% each generation [5, 6]

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# Processor Trends (cont.)

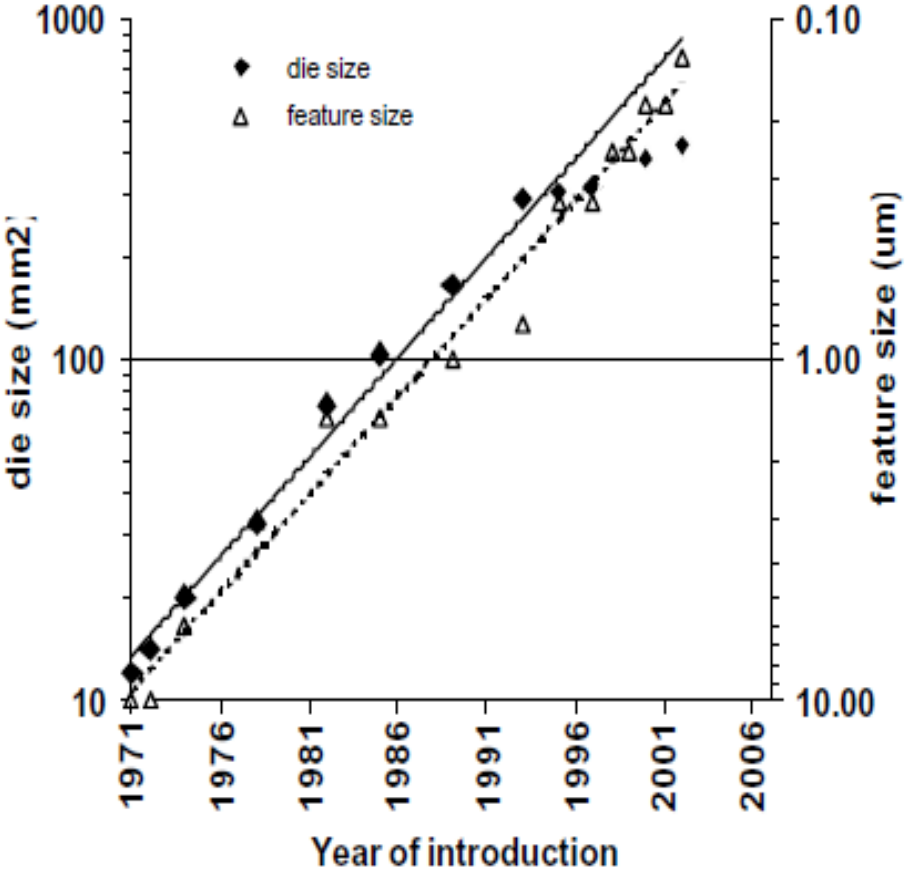


Figure 3 – Feature size reduces by 70% every 2 to 3 years. Die sizes grow at 7% per year [5, 6]

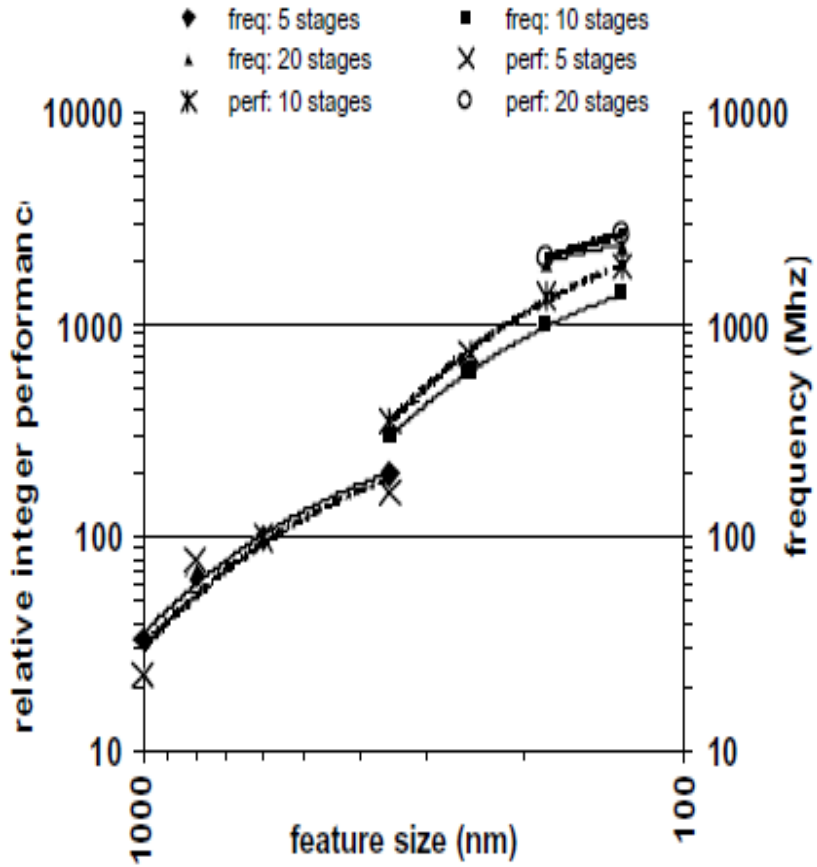


Figure 4 – As feature size gets smaller, longer pipeline enables frequency scaling which is a key driver for performance [5, 6]

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# Processor Trends (cont.)

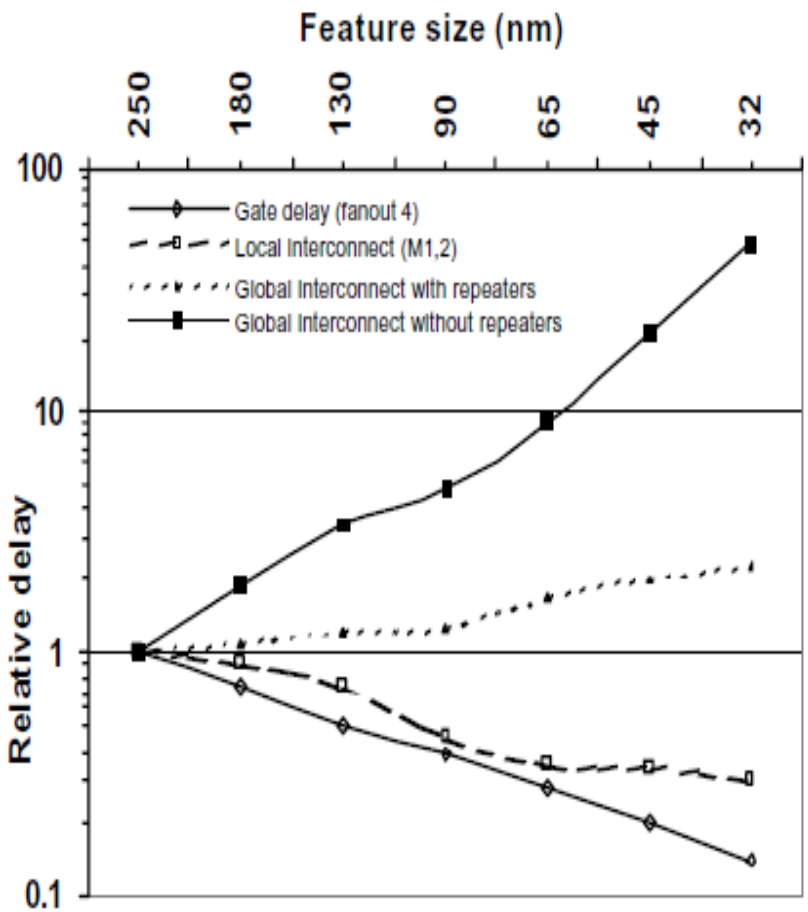


Figure 6 – On-chip interconnect trend [4]

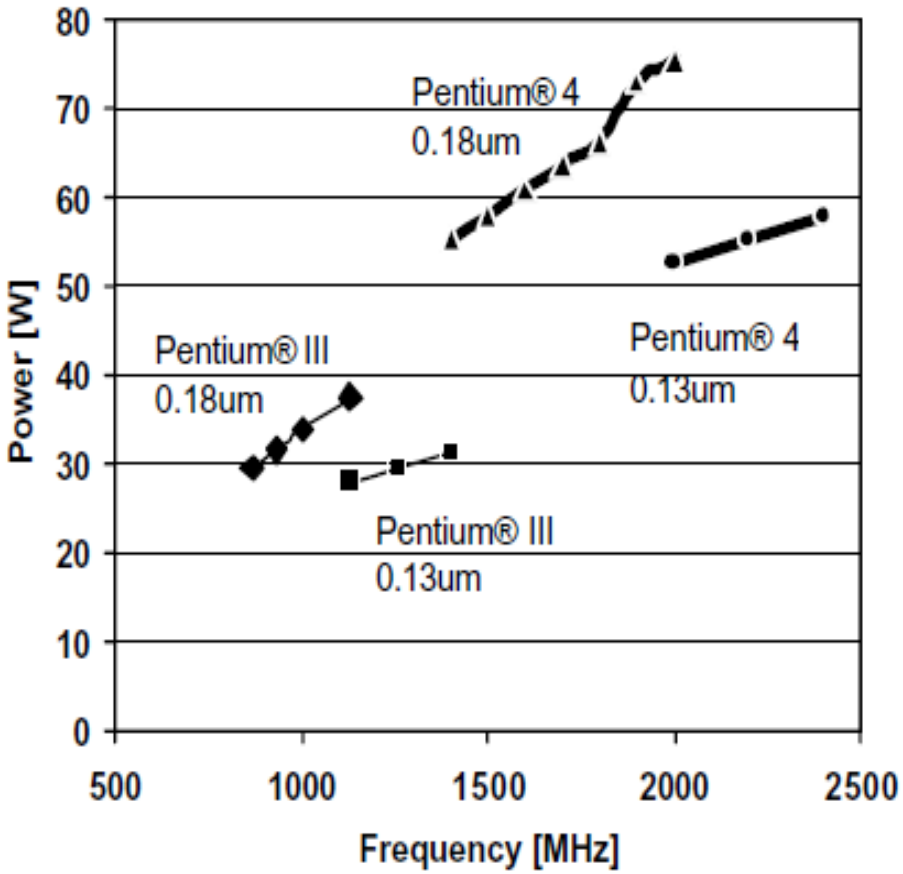


Figure 7 – Processor power as a function of frequency for two process generations [5]

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# Processor Trends (cont.)

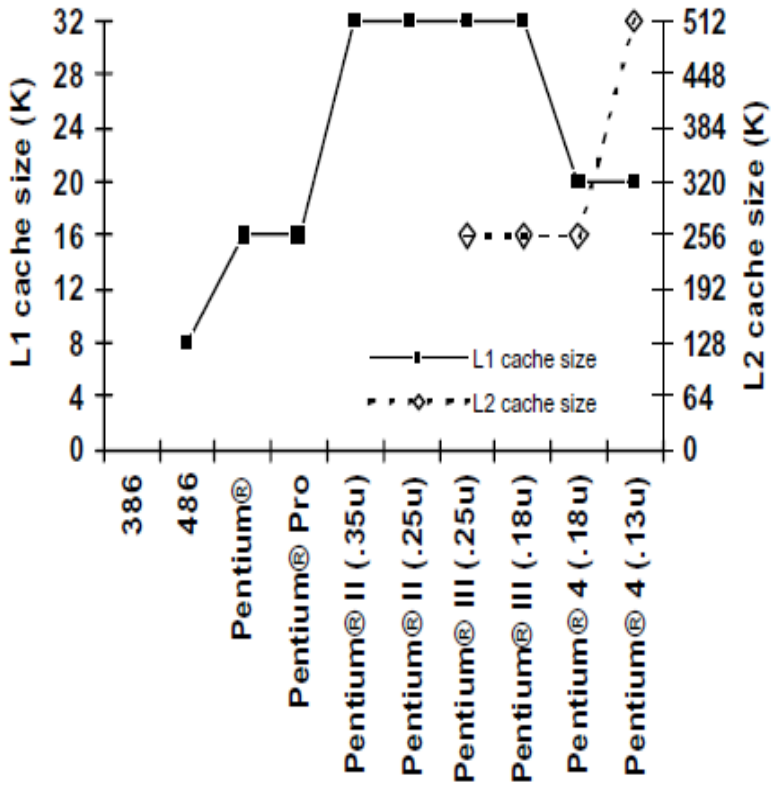


Figure 8 – Increasing on-chip cache sizes reduce the impact of widening processor-memory gap

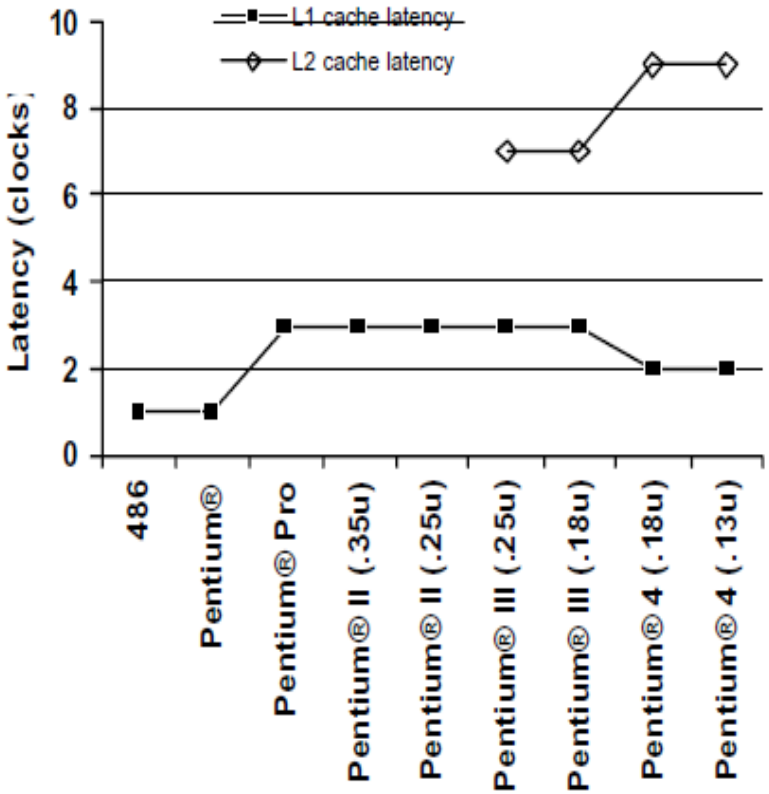


Figure 9 – Short L1 cache latency dictates small L1 cache size. L2 cache latency is less critical and allows larger L2 cache sizes.

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# Processor Trends (cont.)

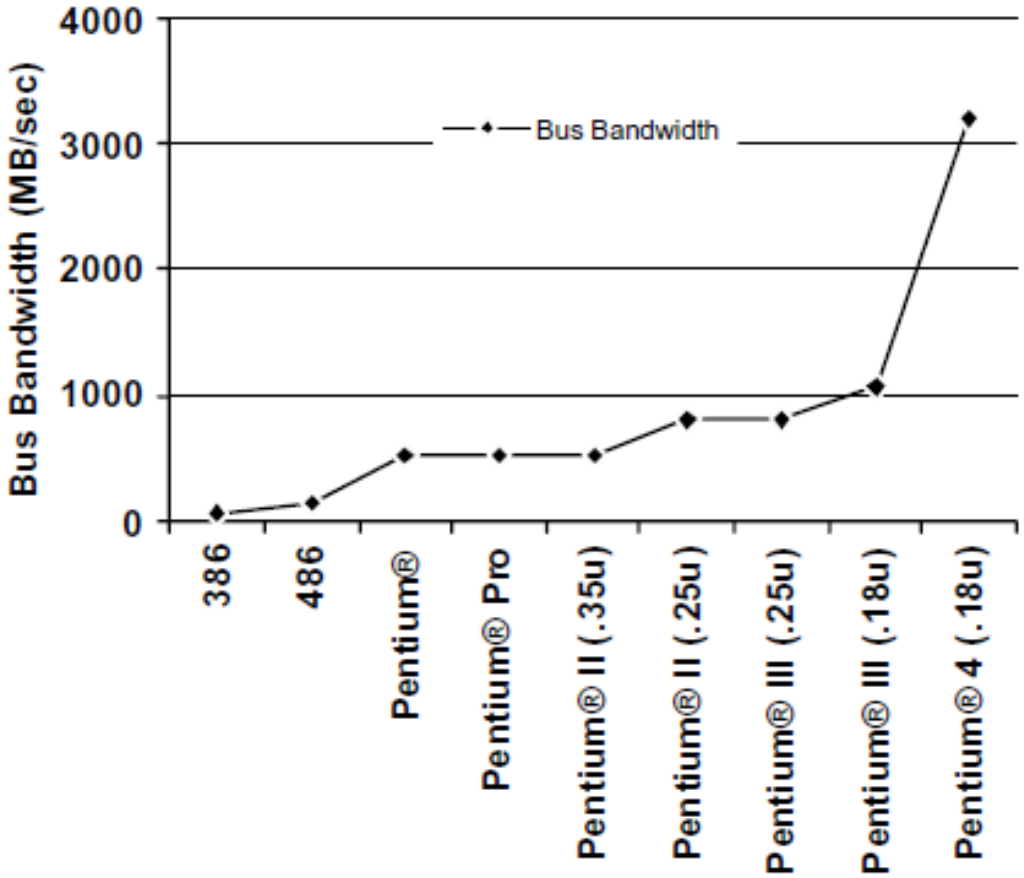


Figure 10 – Memory and I/O bandwidth are crucial to sustain high processor performance

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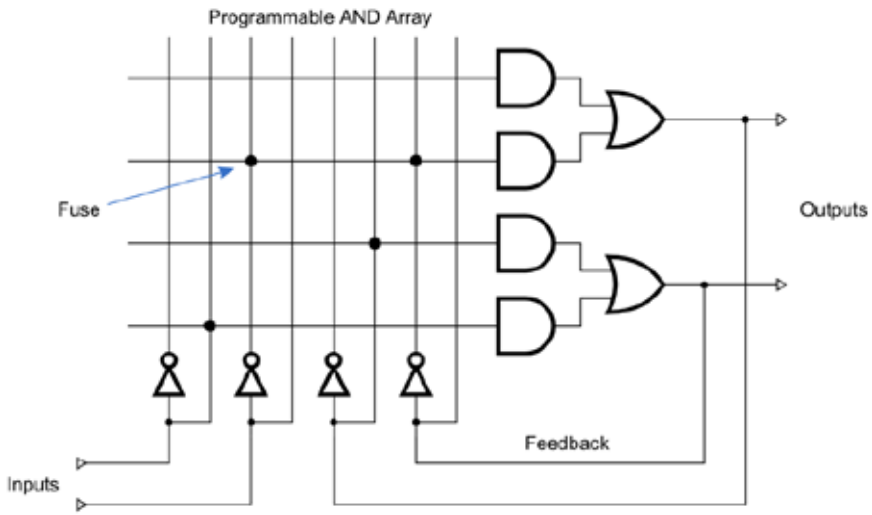
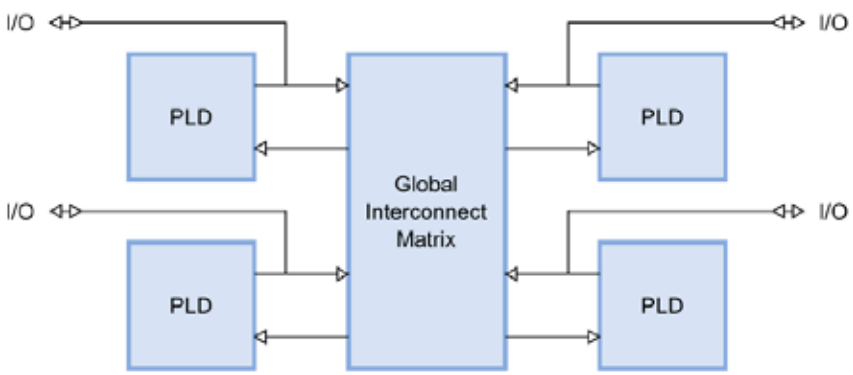
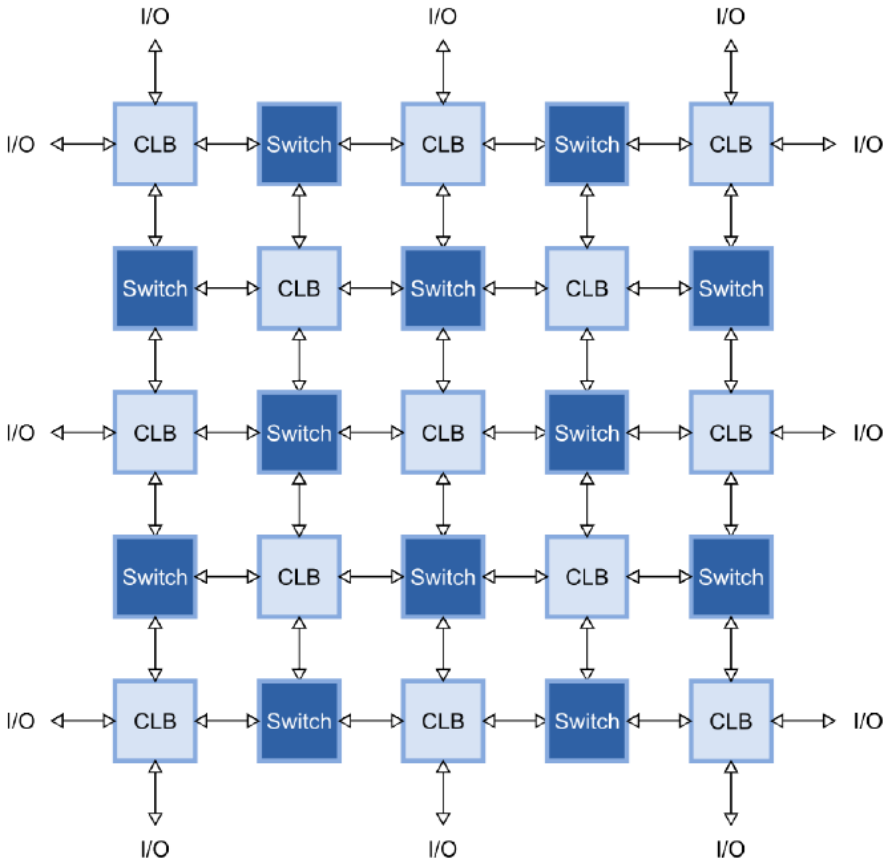
# FPGA Basics

A typical Programmable Logic Device (PLD)




A Complex Programmable Logic Device (CPLD)




FPGAs consist of a matrix of Configurable Logic Blocks (CLBs) and Switches